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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,594	03/30/2004	Seiji Ichiyoshi	02008.106002	4387

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EXAMINER	
KERVEROS, JAMES C	
ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 10/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/813,594	ICHIYOSHI, SEIJI	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9 and 10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9 and 10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a **FINAL OFFICE ACTION** in response to Amendment filed 8/15/2006, which is a continuation-in-part of U.S. patent application No. 10/403,817, filed on March 31, 2003, which is still pending.

Claims 1-9 were previously examined. Claims 1-8 have been cancelled.

Claim 10 is new. Claims 9 and 10 are pending

Objection to the specification has been withdrawn in view of a new title.

The statutory type double patenting rejection under 35 U.S.C. 101, as claiming the same invention as that of claims 1-8 of copending Application No. 10/403,817, has been overcome by having cancelled the conflicting claims 1-8 of the instant Application.

Response to Arguments

Applicant's arguments filed 8/15/2006 have been fully considered but they are not persuasive.

In reference to the rejection of Claim 9 under 35 U.S.C. 102(e), Applicant argues that Bristow fails to disclose any method to flexibly connect test site computers and DUTs, and more specifically, that T/Fs 150 and P/Es 145 in the test site 105-1 cannot be connected with the test site computer of the test site 105-2 because the pin scrambler 155 is not able to set such topology, as illustrated in Figure 3, by Bristow.

In response to Applicant's argument above, the Examiner wishes to direct Applicant's attention to Figure 10, by Bristow, which illustrates a test system 100 comprising multiple test sites 105-1, 105-n linked accordingly, each having a test site

computer 125 linked to together to enable testing of a DUT 110. Any one of the test site computers 125 can be connected with any one of the DUT 110, as described by the example of testing a five-hundred pin DUT 110 by linking eight test sites 105. In the cited example, the computer program selects one of test site computers 125 to control the linked test sites 105-1, 105-n, and for idling the remainder of the test site computers. Clearly, according to the cited example, only one of the eight test site computers 125 is linked to each of the eight test sites 105 required for testing in parallel the five-hundred pin DUT 110, while the remainder seven of the test site computers 125 stay idled. According to Bristow, the computer program also includes program code for synchronizing pattern generators 140 and clocks 135 in each of the test sites 105-1, 105-n to run in parallel.

Therefore, any one of the test site computers 125 can be connected with any of the plurality of DUT 110 located in different test sites 105 for parallel testing.

Furthermore, referring to Figure 9, Bristow discloses an exemplary setup for parallel testing of sixteen 4-pin serial memory devices DUTs, where an operator or test engineer need not write or duplicate a test program for each individual DUT 110. One added line of code per pin is sufficient for test site computer 125 to instruct pin scrambler 155 to apply the same test vector to each DUT 110. Clearly, any test site computer 125 is capable of transmitting the same test vector to each DUT 110 through pin scrambler 155 corresponding to each of the sixteen test sites.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 9 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Bristow et al. (US Patent No. 6,754,868) filed: June 29, 2001.

Regarding Claims 9 and 10, Bristow discloses a test method used for a test apparatus (Figures 3 and 9), including a plurality of test modules (T/Fs 150) coupled to pin electronics (P/Es 145), which are connected to either of the plurality of devices under test (DUT 110), for supplying a test signal from a test signal source or pattern generator 140 to the (DUT 110), and a plurality of control apparatuses (test site computers 125) for controlling the plurality of the (T/Fs 150). Figure 3 is a block diagram of a test system 100 having a single apparatus or test site 105 for testing one or more devices under test (DUT 110), and Figure 9, is an exemplary setup for parallel testing of sixteen 4-pin serial memory devices using a 64-pin test site. The method comprising:

Acquiring a connection switching using a pin scrambling circuit 155 coupled between the pattern generator 140 and the T/Fs 150, which couples any one of the outputs of pattern generator 140 to any one of T/Fs 150, and through the T/F to any one of pins 115 on DUT 110. Thus, the test site 105 enables the output or test signal coupled to a particular pin 115 on DUT 110 to be switched or changed "on the fly" without rewiring of the test site. According to Figure 9, the test signal from (APG 165) is coupled through pin scrambling circuit 155 to T/Fs 150 and PE channels 145 to pins 115 on the DUTs. In Figure 3, one added line of code per pin is sufficient for control apparatus (site computer 125) to instruct pin scrambler 155 to apply the same test vector to each DUT 110. The test site computer 125 is special purpose computer coupled to every other component or element in test site 105 for controlling the operation.

As shown in Figure 10, in the case of the test system 100 comprising multiple computers 125, the computer program selects one of test site computers 125 to control the linked test sites 105-1, 105-n, each having a test site computer 125 associated therewith, and for idling the remainder of the test site computers. The computer program also includes program code for synchronizing pattern generators 140 and clocks 135 in each of the test sites 105-1, 105-n to run in parallel, for testing the plurality of devices under test in parallel.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Date: 3 October 2006
Office Action: Final Rejection

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